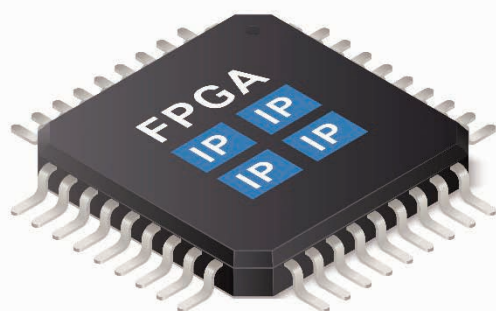# TTTech

^{TTE}End System A664 Core IP

The Certifiable 10/100/1000 Mbit/s TTEthernet® End System IP

Key Benefits

- ✓ RTCA DO-254 DAL A certifiable end system core IP for use in flight programs
- ✓ Fully compliant with Ethernet (IEEE 802.3), rate-constrained (ARINC 664 part 7) and time-triggered traffic (SAE AS6802)
- ✓ Support of 10/100/1,000 Mbit/s on both network and host interface
- ✓ Certification evidence available

^{TTE}End System A664 Core IP is a RTCA DO-254 DAL A certifiable solution which can be used in avionics systems. Modern host interfaces together with a state-of-the-art hardware platform allow the transmission of safety-critical data with up to 1 Gbit/s speeds over avionics data networks, enabling optimization of size, weight and power of the system.

Three traffic classes on one chip

The ^{TTE}End System A664 Core IP supports three traffic classes:
- IEEE 802.3 Ethernet traffic
- ARINC 664 part 7 traffic
- Time-triggered SAE AS6802 traffic with hard real-time guarantee and transport delay jitter in sub-microsecond range

Up to 1 Gbit/s of safety-critical traffic

Two GMII network interfaces together with the high-speed host interface (AXI4) allow the transmission all three traffic classes over the network with up to 1 Gbit/s speeds in a deterministic way. Additionally, the SAE AS6802 traffic class provides fixed transmission latency and jitter in the sub-microsecond range and unmatched bandwidth efficiency while maintaining full determinism (up to 95% utilization of available network bandwidth). GMII interfaces (in possible triplication mode) allow the

integration of ^{TTE}End System A664 Core IP in dual fault-tolerant networks.

Diagnostic and health monitoring

The ^{TTE}End System A664 Core IP contains self-diagnostic and health monitoring capabilities such as configuration and frame memory protection mechanisms, configurable scrubbing rates, continuous Built-In Tests, etc. All these allow the use of the IP in different environmental and radiation conditions.
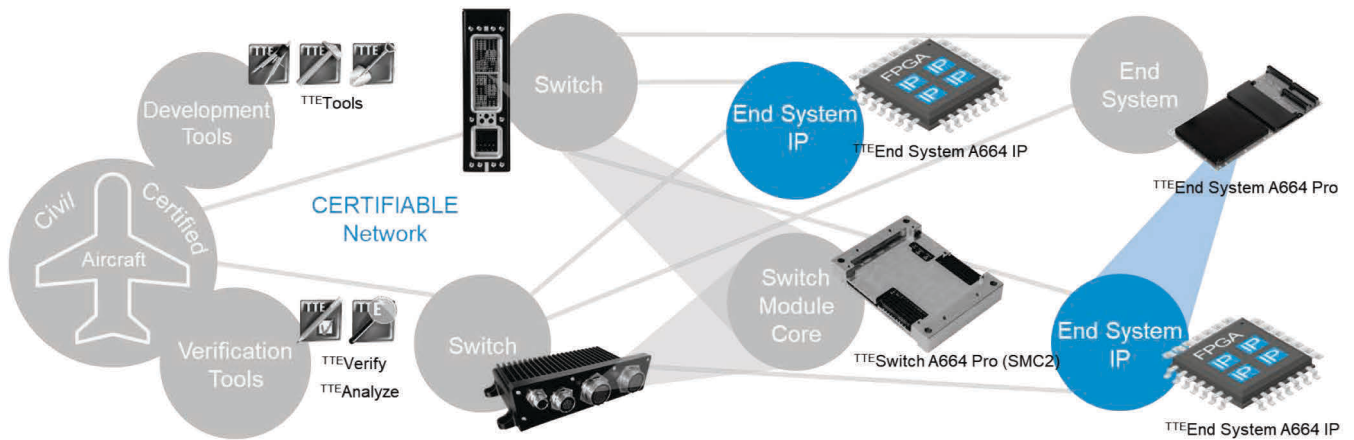
SWaP optimization

The possibility to utilize MPSoC platforms allows the integration of the ^{TTE}End System A664 Core IP solution on high circuitry density PCBs. This provides flexibility in the hardware design and leads to significant SWaP improvements.

Application Fields

- Technology evaluation
- Architecture development
- Flight programs

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General product features	- IP size is ~45,000 LUTs (Xilinx US+ Device Family) 256 Tx VLs 512 Rx VLs 2,048 Tx ports 4,096 Rx ports - Host interface: AXI4, 32-bit at 125 MHz - Network interface: supports two GMII channels
Standards compliance	- IEEE 802.3 - ARINC 664 part 7 - SAE AS6802
Documentation	^{TTE}End System A664 Core IP user manual - Errata sheet - Release notes - Programmers' manual - IP design and integration guide - DO-254 certification package (optional) ^{TTE}End System Core IP PHAC ^{TTE}End System Core IP HRD ^{TTE}End System Core IP HDD ^{TTE}End System Core IP HCI ^{TTE}End System Core IP HECI ^{TTE}End System Core IP HTI ^{TTE}End System Core IP HVCP ^{TTE}End System Core IP HVR ^{TTE}End System Core IP HAS
Drivers (non-certified)	- BareMetal driver - Other drivers based on request
Order number	Available on request

products@tttech.com   www.tttech.com