Arion IP Evaluation Platform

World's 1st Ethernet Switch with ARINC 664 part 7, IEEE TSN and SAE AS6802

Key Benefits

- Demonstrates Ethernet switch IP core technology with IEEE TSN, ARINC 664 part 7, SAE AS6802
- Offers mixed operation and the capabilities of different Ethernet services integrated on one device
- Enables evaluation of complete hardware and software package with pre-installed switch configuration GUI tool
- Contains configurable Ethernet IP and scalable features for FPGA and silicon designs
- Availability: Q2 / 2021

TTTech Aerospace's Arion IP Evaluation Platform is an Ethernet switch IP core technology demonstrator based on our proven aerospace Ethernet switch IP designed for critical, integrated applications in the aerospace sector. This IP integrates best-effort, real-time and hard real-time Ethernet traffic, while processing Ethernet frames deterministically and with known latency. The Arion IP enables full compliance with ARINC 664 part 7 standard virtual links (VLs), synchronous and low-jitter VLs (SAE AS6802), and IEEE TSN protocols (802.1Qci, 802.1CB, 802.1Qbv, 802.1AS). A flexible and user-friendly switch configuration tool is included.

IEEE 802.1AS and IEEE 1588 v2 Time Synch

Profile of IEEE 1588 v2 for synchronization of clocks in the network. Supports timing requirements for scheduled TSN networks with gPTP / 802.1AS, and TC P2P. Provides guaranteed communication latency for time-critical traffic over standard Ethernet even in a converged infrastructure.

IEEE 802.1Qci Filtering and Policing

Protects against faulty and/or malicious endpoints and switches. Isolates faults to specific regions in the network.

IEEE 802.1CB Seamless Redundancy

Enables seamless redundancy for increased network availability. Allows for redundancy on a per stream basis for individual critical streams.

ARINC 664 part 7 VLs and Traffic Policing

Enables integration of legacy devices with ARINC 664 interfaces without congestions, packet delays and interferences.

SAE AS6802 synchronization and synchronous VLs

Enables strict determinism and guaranteed non-interference for the most demanding integrated modular architectures.

Legacy Best-Effort Traffic Configured for Real-time Applications

Enables integration of legacy devices with Ethernet interfaces without congestions.

Potential Application Fields

- Aerospace
- Space
- UAM/UAV

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Arion IP Features

Ports	Max. 11 ports with 10/100/1000 Mbit/s or 1-2.5 Gb/s; max. 2x 2.5 Gb/s
IP interfaces	MII, GMII, RMII, RGMII, SGMII gPTP Pulse-Driven Synchronization
TSN	IEEE 802.1AS Time Synchronization supported in IP IEEE 802.1Qbv Scheduled Traffic IEEE 802.1Qci Filtering and Policing IEEE 802.1CB Frame Replication and Elimination
AVB	IEEE 802.1AS Time Synchronization for Time-Sensitive Applications (gPTP) supported in IP IEEE 802.1Qav Forwarding and Queuing for Time-Sensitive Streams (FQTSS) IEEE 802.1Qat supported in IP
SAE AS6802	Time-triggered Ethernet with scheduled time-triggered packet forwarding
ARINC 664 part 7	Deterministic data transfers in a network for safety-critical aerospace applications
Partitioned best-effort traffic (designed-in non-interference)	Legacy endpoint traffic can be configured as full TSN-like quality of service with total isolation and non-interference
IEEE 802.1Q	Port-based VLANs and VLAN tagging Prioritization of packets on egress ports Tagging/Untagging of VLAN frames on ingress/egress ports Line Speed Retagging
Clock synchronization	IEEE 802.1AS support SAE AS6802 synchronization IEEE 1588-2008 layer 2 one-step P2P TC transparent clock support
Switching engine	Store and forward architecture with full cross-sectional non-blocking bandwidth of 8 Gb/s 256 kB frame buffer IPv4/IPv6 routing supported in ASIC variant (based on 128 Byte entries) 4096 VLANs Up to 1024 entry MAC address hash/CAM (FPGA) or TCAM (ASIC)-based learning table Up to 4096 stream/flow policers per switch Up to 1024 MAC address filters 80 asynchronous traffic shapers (CBS) per switch Red, Yellow, Green traffic classes MEF 10.3 (QCI) Static and dynamic configuration of MAC addresses Flow identification-based MAC addresses Ingress rate-limiting on a per-port and per-MAC unicast, multicast, and broadcast traffic (supported on two ports in Evaluation Platform FPGA) VLAN Mirroring Virtual Switch Management (2-4 switches can be configured to operate as one switch)
FPGA limitations	The Evaluation Platform Arion IP is hosted on a FPGA board; compared to the full Arion IP capabilities listed above, it has the following limitations: • xMII, ext. interfaces are RMII only, 4 ports (100/1000 Mb/s) supported in the evaluation platform • 64 MAC addresses • 32 CBS shapers for AVB • Packet Inspection TCAM entries are limited to 32 entries and 16 Byte depth • Max. 1 Gb/s line bandwidth Please contact us for further modification and customization possibilities.
Software	Ethernet Switch Configuration Tool
Product number	13744

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