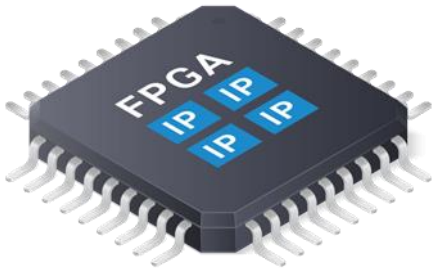
Ensuring Reliable Networks TTTech

TTEEnd System A664 Pro (FPGA)

The Certifiable 10/100/1000 Mbit/s TTEthernet Network End System IP



Key Benefits

- RTCA DO-254 DAL A certifiable End System IP for use in flight programs
- Fully compliant with Ethernet (IEEE 802.3), rate-constrained (ARINC 664 part 7) and time-triggered traffic (SAE AS6802)
- Configurable to optimize integrator's solution
- Certification data evidence available

The TTEEnd System A664 Pro (FPGA) brings the full power of deterministic Ethernet communication technology to aerospace certifiable hardware. TTEthernet technology enables hard real-time operation in distributed systems based on Ethernet networks with speeds up to 1Gbit/s. The End System solution uniquely supports three standard traffic classes: Ethernet (IEEE 802.3), rate-constrained (ARINC 664 p7) and time-triggered (SAE AS6802) traffic in parallel on one physical media.

End System Function

TTEEnd System A664 Pro (FPGA) is a deterministic Ethernet end point solution on an FPGA enabling the implementation of critical network-centric applications. It provides dual channel gigabit communication over the Ethernet network while performing traffic shaping using three traffic classes (Best Effort, Rate Constrain, Time Triggered). It guarantees latency within 150us regardless of frame size and supports Time-Triggered Ethernet synchronization.

TTEEnd System A664 Pro (FPGA) supports the transmission time-critical and safety-critical data according to a predefined schedule, not affected by the number of application streams on the channel, or by traffic bursts.

Configurability

TTEEnd System A664 Pro (FPGA) solution provides pin strapping interface to enable/disable features to optimize resources, performance and dependability as required in the target installation. Key configurability items are host connectivity protocols, network interface configurations, bandwidth support, security and soft error mitigation management.

Certifiability

TTEEnd System A664 Pro (FPGA) is developed in accordance to DO-254 DAL A and builds on top of the certifiable TTEEnd System A664 Core IP Pro solution. A complete lifecycle evidence data set is available to support the integrator in the certification activities with its OEM and Airworthiness Authority.

Application Fields

- Aircrafts
- Rotorcrafts
- UAV/UAM

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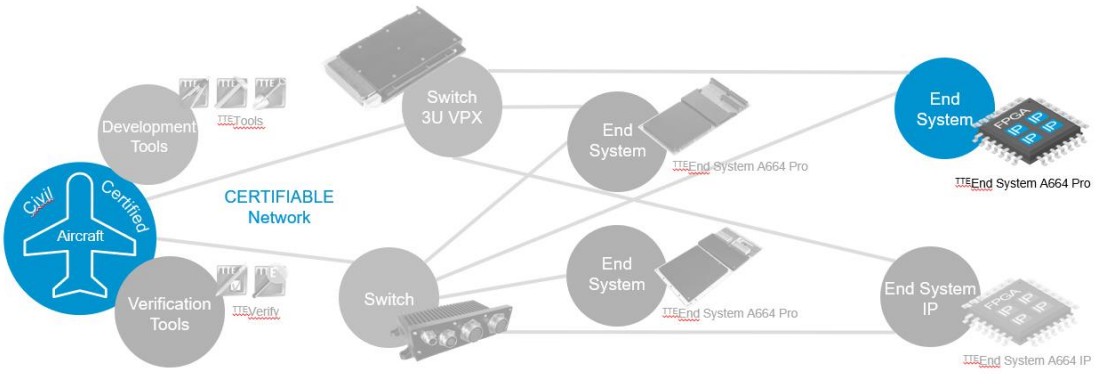

End System Capabilities	– Dual channel gigabit Ethernet communication – Configurable Ethernet traffic classes: ✓ Time-triggered traffic (synchronous, deterministic) ✓ Rate-constrained traffic (asynchronous, deterministic) ✓ Best effort traffic (asynchronous, non deterministic) – 256 send VLs, 2048 receive VLs, 1024 send ports, 4096 receive ports – Up to 8 application partitions supported (IP source address) – Flexible configurable periods (us granularity) – Profiled IP/UDP, sampled and queued COM port network interfaces, handled in hardware ✓ Limitless number of ports configured per VL – 2 output/input memory partitions/access points
Certifiability	– RTCA DO-254 DAL A as certification base, compliance to EASA AMC 20-152A and AMC 20-189
Supported Standards	– IEEE 802.3 – ARINC 664 part 7 – SAE AS6802
Configurability	– Host CPU interface: PCIe / SPI – Ethernet SGMII PHY: Hard coded / externally loaded – Host interface operation mode: DMA / Direct – Essential bit classification: – SEM IP monitoring: Status Interface / UART – SEM IP Clock: 125/200 MHz – PCIe/SPI limited access mode: enable / disable – Debug mode: enable / disable
Packaging	– IP delivered as bitstream for target FPGA Xilinx Artix US+ AU25P
Power Consumption	– 6.2 W max @ FPGA junction temperature +90C.
Driver Support	– Linux 32/64-bit with Kernel >= 3.10 – DO-178C Certifiable RTOS package: on request
Tools Support	– TTETools Development Suite – for device configuration creation – TTEVerify (DO-330 qualified tool) - for device configuration verification
Documentation	– Hardware integration manual – Reference design – Release notes – Errata / Problem reports – DO254 DAL A Certification Data Package
Order Number	– 14572

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