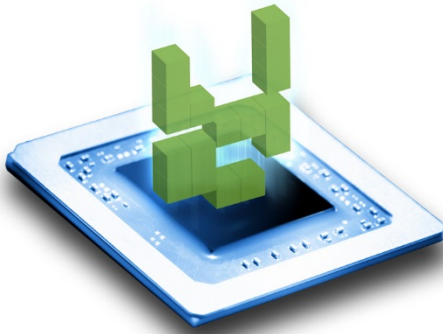




# DEIP Solution Edge

3/5 Port Deterministic Ethernet IP Solution with TSN (Time-Sensitive Networking)



## Key Benefits

- ✓ Compact solution for fast and easy integration into planned and existing FPGA-based devices
- ✓ Provides guaranteed low-latency communication for critical traffic
- ✓ Includes the latest IEEE 802.1 Ethernet standards
- ✓ Seamless compatibility with TTTech Slate XNS network scheduler and topology builder

TTTech's Edge IP Solution is the simple way to add TSN (Time-Sensitive Networking) Ethernet functionality to switched endpoint devices such as industrial controllers. Edge IP Solution includes IP core and associated software for fast and easy integration onto your FPGA enabling open, standard deterministic switching functionality.

## TSN Switching

### Standards Support

Edge IP Solution supports the core TSN mechanisms of time-synchronization (IEEE 802.1AS) and traffic scheduling (IEEE 802.1Qbv) as well as other mechanisms such as frame preemption (IEEE 802.1Qbu) and cut-through.

### Network Scheduling

Edge IP Solution combines with TTTech Slate XNS software to make building topologies, creating schedules and deploying configurations for TSN networks easy. TTTech's high performance scheduling engine is built in to the Slate XNS software for scheduling of IEEE 802.1Qbv and 802.1Qbu traffic as well as cut-through data streams.

## Ease of Integration

### Configurable Design Block

The Edge IP Solution Qsys component enables users to choose from a range of xMII interfaces and other system parameters. IP features can be adapted to find the right balance between size and functionality, resulting in an optimal footprint for your application. Interconnect logic between IP functions and subsystems can be automatically generated to save time and effort in FPGA design.

### Evaluation

A reference design for the Edge IP Solution is available. Together with NovTech's NetLeap Evaluation Kit it provides an easy to use platform for evaluating Edge IP Solution features on Altera Cyclone V SoC.



## Application Fields

- Factory Automation
- Process Automation

## IP Solution Delivery

- Encrypted Qsys IP component including interface adapters to xMII
- Software and device drivers for Linux
- Reference design for NovTech NetLeap board
- Getting started guide
- Technical documentation

## Product Features

Ports	3 to 5 ports; 10/100/1000 Mbit/s
Target Device	Altera Cyclone V SoC
Physical Interfaces	MII, GMII PPS (Pulse-Per-Second) output Avalon slave interface for management register access
Reference Design Adapters	MII, GMII, RMII, RGMII, SGMII, 100BASE-FX, 1000BASE-X
TSN	IEEE 802.1AS Time Synchronization IEEE 802.1Qbv Scheduled Traffic IEEE 802.1Qbu Frame Preemption
IEEE 802.1Q	Port-based VLANs and VLAN tagging Assignment to traffic class on ingress ports Forwarding and Queuing for time-sensitive streams
Clock Synchronization	IEEE 802.1AS IEEE 1588-2008 layer 2 one/two-step end-to-end transparent clock support
Configuration	Netconf 1.0/1.1 (RFC 6241) including derived YANG models - IEEE 802.1Qbv Scheduled Traffic - IEEE 802.1Qbu Frame Preemption - IEEE 802.1Qcp Bridges and Bridged Networks (VLAN support) SNMP v1/v2 (RFC 3416) including MIB
Switching Engine	Store and forward architecture providing full cross-sectional bandwidth 128 Kbit frame buffer per port 4096 VLANs 16 MAC address filters per port Up to 4096 entry MAC address hash based learning table Up to 4096 policers per port 8 traffic shapers per port (optional) Static configuration of MAC addresses Flow identification based MAC addresses Ingress rate-limiting on a per-port basis for unicast, multicast, and broadcast traffic
Operating System	Linux Kernel 4.9 LTS, LTSI (optional real-time patch) Support for Linux net_dev, switch_dev, and PHC (PTP hardware clock)
Embedded Software Stacks	IEEE 802.1AS Time Synchronization IEEE 1588-2008 2-step and 1-step master and slave functionality RSTP (Rapid Spanning Tree Protocol) support for best-effort (IEEE 802.1Q-2014)
Product number	12643



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