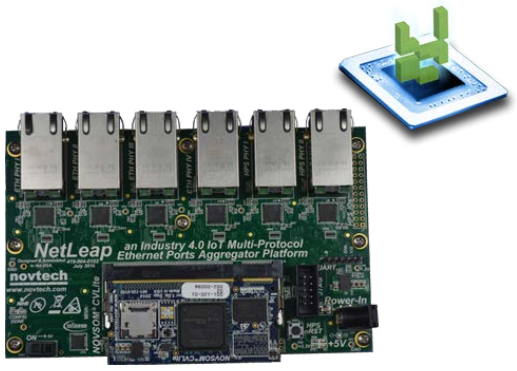
Ensuring Reliable Networks TTTech

DEIP Solution Edge - Reference Design

Evaluate IEEE TSN (Time-Sensitive Networking) Ethernet on NetLeap



Key Benefits

- Fast and easy set-up for evaluating IEEE TSN on FPGA
- Provides guaranteed low-latency communication for critical traffic
- Includes the latest IEEE 802.1 Ethernet standards

TTTech's DEIP Solution Edge - Reference Design combines with NovTech's NetLeap Evaluation Kit to provide an easy to use platform for evaluating IEEE TSN Ethernet on Intel Cyclone V SoC. NetLeap can be used with the Edge IP Solution Reference Design to support the development of TSN enabled switches or endpoints.

Edge IP Solution Reference Design

Includes:

- Encrypted DEIP Solution Edge source code (including support for IEEE 802.1Qbv Scheduled Traffic and IEEE 802.1AS Time Synchronization
- IEEE 1588-2008 2-step and 1-step master and slave functionality
- Device drivers for Linux (net_dev/switch_dev support) (other OS on request)
- Additional standards will be added in accordance with the DEIP Solution Edge roadmap

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NetLeap Evaluation Kit

Includes:

- NOVSOM®CVL Intel Cyclone V SoC
- NetLeap base board
- 6x 1GbE ports (2 connected to ARM Cortex-A9 core, 4 to FPGA fabric)
- SD card with Linux image and example code
- UART TTL to USB cable
- USB drive with manuals, documentation, quick start guide and Virtual Machine
- Power supply

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Application Fields

- Factory Automation
- Process Automation

Edge IP Solution Features

Ports	3 to 5 ports; 10/100/1000 Mbit/s
Target Device	Altera Cyclone V SoC
Physical Interfaces	MII, GMII PPS (Pulse-Per-Second) output Avalon slave interface for management register access
Reference Design Adapters	MII, GMII, RMII, RGMII, SGMII, 100BASE-FX, 1000BASE-X
TSN	IEEE 802.1AS Time Synchronization IEEE 802.1Qbv Scheduled Traffic IEEE 802.1Qbu Frame Preemption
IEEE 802.1Q	Port-based VLANs and VLAN tagging Assignment to traffic class on ingress ports Forwarding and Queuing for time-sensitive streams
Clock Synchronization	IEEE 802.1AS IEEE 1588-2008 layer 2 one/two-step end-to-end transparent clock support
Configuration	Netconf 1.0/1.1 (RFC 6241) including derived YANG models - IEEE 802.1Qbv Scheduled Traffic - IEEE 802.1Qbu Frame Preemption - IEEE 802.1Qcp Bridges and Bridged Networks (VLAN support) SNMP v1/v2 (RFC 3416) including MIB
Switching Engine	Store and forward architecture providing full cross-sectional bandwidth 128 Kbit frame buffer per port 4096 VLANs 16 MAC address filters per port Up to 4096 entry MAC address hash based learning table Up to 4096 policers per port 8 traffic shapers per port (optional) Static configuration of MAC addresses Flow identification based MAC addresses Ingress rate-limiting on a per-port basis for unicast, multicast, and broadcast traffic
Operating System	Linux Kernel 4.9 LTS, LTSI (optional real-time patch) Support for Linux net_dev, switch_dev, and PHC (PTP hardware clock)
Embedded Software Stacks	IEEE 802.1AS Time Synchronization IEEE 1588-2008 2-step and 1-step master and slave functionality RSTP (Rapid Spanning Tree Protocol) support for best-effort (IEEE 802.1Q-2014)

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