Ensuring Reliable Networks TTTech

TTP Simulate XMC/PCIe

The High-Performance TTP Test System

Key Benefits

- Real-time simulation board
- Simulation of up to 4 TTP nodes
- Full tools support
- Driver support for Linux and Windows®
- PCIe and XMC form factor
- IRIG-B time stamping
- Simple, high-level API

TTP Simulate is a high-performance test system which enables the simulation of a networked TTP® system in real-time. It allows full hardware in the loop verification of a TTP unit. There are two form factors available for this product – PCIe and XMC card format. Both cards can act as four independent TTP nodes and have an IRIG-B interface for time stamping. Both versions support TTP classic speed with a 4 Mbit/Manchester physical layer and TTP high-speed 20 Mbit/8B10B physical layer.

Simulation of a Real-Time TTP System

One or more TTP Simulate cards can be plugged into the PCIe sockets of a PC. Every card represents several TTP nodes. TTP Simulate is controlled by the main CPU of the computer to which the card has been deployed. The interface between the embedded CPUs and the main CPU is a dual ported RAM (DPRAM). All messages received are available in the DPRAM. The simulation on the main CPU accesses the DPRAM on the hardware component through the client API and the PCI driver. Thus, a networked TTP real-time system can be simulated without setting it up in expensive flight hardware or customized hardware. This results in considerable cost reductions and shorter development and test cycles.

Embedded Software Package

TTP Simulate includes an embedded software package. The embedded software is executed on the embedded CPUs. It interfaces with the TTP controller and places the data from the TTP bus in the DPRAM. The embedded software is configured using the software tool TTP Simulate Setup. It enables the user to specify which messages will be provided in the DPRAM of the hardware component.

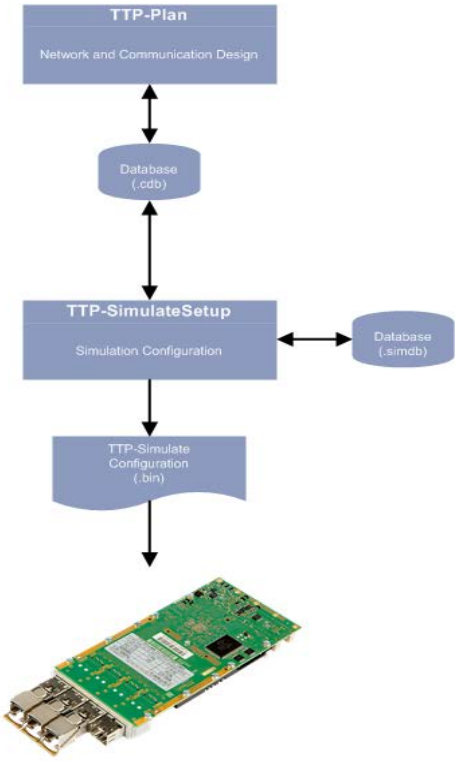
The client API running on the main CPU provides high level access to the DPRAM. The client API is available for Windows® and Linux.

Application Fields

- Technology Evaluation
- Product Testing
- Architecture Development

Related Products

The TTPSimulate Setup tool is needed to configure the TTPSimulate board. The tool takes the configuration of the network from TTPPlan as input. The user provides additional information about the desired test and simulation setup. Based on the input, TTPSimulate Setup creates the configuration files for the boards.



Physical Layer	Front connectors: exchangeable SFP modules − 1 x SFP for 4 Mbit MFM/Manchester on RS 485 physical layer − 1 x SFP for 20 Mbit 8B10B on RS 485 physical layer − 1 x SFP for IRIG-B
Environmental Operating Ranges	Lab environment Conduction cooling Operating temperature: 0 °C to +70 °C Storage temperature: -40 °C to +85 °C Operating/non-operating humidity: humidity level from 25% to 90%
Power Requirements	+12 V supply from J15 connector +3.3 V Supply from J15 connector +12 V or +5 V over VPWR from J15 available on request
Dimensions	170 x 75 (mm)
Weight	200 g
Form Factor	IEEE 1386.1-2001 PMC 149 x 74 (in mm) Vita 42 Conduction Cooled XMC with faceplate I/O Conduction cooled board design Host interfaces: PCIe 1.1 x 4 Gen1 (2.5 Gbit/s)
Order Number	12029: TTPSimulate XMC incl. 1 single-seat license for TTPSimulate Setup 12030: TTPSimulate PCIe incl. 1 single-seat license for TTPSimulate Setup 12031: TTPSimulate PCIe incl. 1 single-seat license for TTPSimulate Setup (without SFPs) 12012: TTPSimulate Setup configuration tool 12036: Additional standard speed SFP 12037: Additional high speed SFP 12038: SFP IRIG B module

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