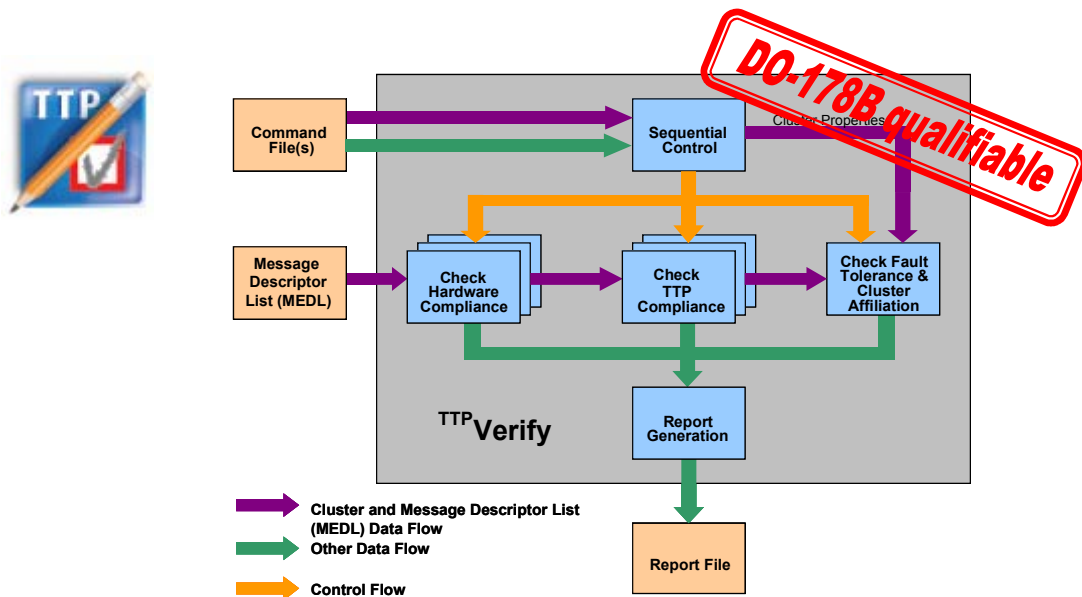


TTTech Verification Tool



TTPVerify – The DO-178B Qualified TTP Design Verification Tool

TTPVerify is a comprehensive tool for the verification of TTP cluster designs. It is qualified and designed in compliance with the RTCA software standard DO-178B Level A as a Verification Tool. This is a prerequisite for supporting the development of safety-critical distributed real-time systems for automotive and aerospace applications. The role of this tool in the design process is to detect and automatically analyze faults of cluster designs. As a result, major savings are possible early in the design process by significantly reducing expensive review iterations during the verification and test phases.

Verification of the Message Descriptor List

A TTP cluster contains a number of hosts exchanging messages in a statically defined temporal pattern. Any TTP controller in the cluster has stored this temporal pattern in its communication schedule. The message descriptor list (MEDL) defines the entire transmission behavior on the bus and the behavior of the local communication network interface (CNI) to the host controller and thus influences safety behavior, redundancy, and fault tolerance properties. TTPVerify also checks the position of the MEDLs inside the TTP communication controllers along with other target-specific constraints.

Verification of Communication Requirements Traceability into the Schedule

In a tool-supported development process a scheduling tool such as TTP-Plan is used to derive a TTP communication schedule automatically from communication requirements specified by the user. In order to verify, that all communication requirements are correctly implemented in the MEDLs of each communication controller in the system, TTP-Verify checks that all configuration parameters found in the binary MEDLs actually match the users's requirements and certifies their correctness or reports any mismatches.

The output of TTPVerify is a file that is divided into chapters for better readability. To allow a condensed view of the verification results, the user is able to customize the report to his needs. The user cannot influence the verification algorithms to avoid conditions where the tool may fail due to erroneous TTP cluster design data. TTPVerify is built to detect design and implementation errors in an early phase of the development cycle. This substantially increases safety and reduces development costs. TTPVerify seamlessly integrates with TTTech's 6th generation of the TTPTools software development environment.

General Features

- Checks the MEDL compliance with TTP requirements
- Checks the MEDL compliance with the controller requirements
- Checks the affiliation of different MEDLs to the same cluster
- Verifies the correct traceability and correct implementation of communication requirements in MEDLs
- Checks the fault tolerance of the cluster design
- Designed for highest safety requirements
- Easy to integrate in development tool chains
- Easy automation via command file interface
- Detailed and customizable output of the verification results
- Supports the austriamicrosystems AS8202NF (C2NF) TTP communication controller
- Developed as a RTCA/DO-178B Verification Tool

System Requirements

- Microsoft Windows 2000, or Windows XP (support for other operating systems is available upon request)
- ^{TTP}Plan for MEDL generation, TTP schedule generation and checking
- ^{TTP}Load for MEDL download and MEDL extraction

Subject to changes and corrections.

For further information, including price and availability, contact products@tttech.com.

TTP is a registered trademark of FTS Computertechnik Ges.m.b.H. TTP-Tools, TTP-Plan, TTP-Load, and TTP-Verify are product names of TTTech Computertechnik AG. All other trademarks are the property of their respective holders. To the extent possible under applicable law TTTech Computertechnik AG hereby disclaims any and all liability for the content and use of this preliminary data sheet.