Application Note: AN D-151-AN-05-002 **Revision:** 1.1
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Application Note D-151-AN-05-002

Subject

This application note affects the AS8202NF TTP Communication controller datasheet revision 2.1 and prior. AS8202NF PLL lock detection circuitry indicates unjustified PLL-unlock signal and sets AS8202NF into FREEZE STATE.

Description

According to the datasheet rev. 2.1 an earlier, the AS8202NF Communication Controller supports two main clock operation modes: 10MHz (crystal or oscillator) and 40 MHz oscillator. In some cases, the operation with enabled PLL, the TTP controller can switch into FREEZE STATE. This affects all applications that use the internal AS8202NF PLL circuitry with the PLLOFF pin connected to Vss.

This problem happens more often, when

- a random or transient jitter in the range of a few hundred picoseconds at the main oscillator input XIN0 is applied; this causes the PLL lock detection circuitry to generate a PLL-unlock signal that brings the AS8202NF into FREEZE STATE.
- a voltage ripple in the range of a few tenth millivolts on the 3.3V main supply voltage causes the same behavior like described prevously.
- operating the AS9202NF at low temperatures.

Solution

Use a 40MHz main oscillator and disable the PLL by connecting the PLLOFF pin to Vdd. Thus, 10 MHz crystal and oscillator modes must not be used and are no more supported. In particular, this means the following pinning must be used:

Pin Name	Pin Number	Description
XIN0	2	40 MHz oscillator
XOUT0	3	Do not connect
PLLOFF	23	VDD

The clock of the bus guardian (XIN1, XOUT1) is not affected from this application. The described solution is reflected in the AS8202NF datasheet V2.2

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APPLICATION ANALYSIS

If the AS8202NF TTP Controller is not used as described in this document, an analysis of the application behavior can be performed to handle potential safety issues. Please contact TTTech to support you in this analysis.

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