Title: AS8202NF (TTP/C-C2NF controller) Connected to MII Transceiver

Description:

Circuit Description of the AS8202NF

The AS8202NF communication controller is an integrated device supporting serial communication according to the TTP® specification version 1.1. It performs all communication tasks such as reception and transmission of messages in a TTP cluster without interaction of the host CPU. TTP provides mechanisms that allow the deployment in high-dependability distributed real-time systems. It provides the following services:

- Predictable transmission of messages with minimal jitter
- Fault-tolerant distributed clock synchronization
- Consistent membership service with small delay
- Masking of single faults

The CNI (communication network interface) forms a temporal firewall. It decouples the controller network from the host subsystem by use of a dual ported RAM (CNI). This prevents the propagation of control errors. The interface to the host CPU is implemented as a 16-bit wide non-multiplexed asynchronous bus interface.

TTP follows a conflict-free media access strategy called time division multiple access (TDMA). This means, TTP deploys a time slot technique based on a global time that is permanently synchronized. Each node is assigned a time slot in which it is allowed to perform transmit operation. The sequence of time slots is called TDMA round, a set of TDMA rounds forms a cluster cycle. The operation of the network is repeated after one cluster cycle. The sequence of interactions forming the cluster cycle is defined in a static time schedule, called message descriptor list (MEDL). The definition of the MEDL in conjunction with the global time determines the response time for a service request.

The membership of all nodes in the network is evaluated by the communications controller. This information is presented to all correct cluster members in a consistent fashion. During operation, the status of all other nodes is propagated within one TDMA round.

TTP/C Bus Interface

The AS8202NF contains two TTP bus units, one for each TTP channel, building the TTP bus interface. Each TTP bus channel contains a transmitter and a receiver and can be configured to be either in the asynchronous or synchronous mode of operation. Note that the two channels (channel 0 and channel 1) can be configured independently for either of these modes.

The drivers of the TXD and CTS pins are actively driven only during a transmission window, all the other time the drivers are switched off and the weak pull resistors are active. External pull resistors must be used to define the signal levels during idle phases. Note that the transmission window may be different for each channel.

Pin Name	TX inactive
TXD[0]	weak pull-up
CTS[0]	weak pull-down
TXD[1]	weak pull-up
CTS[1]	weak pull-down

TTP/C Asynchronous Bus Interface

When in asynchronous mode of operation the channel's bus unit uses a self-clocking transmission encoding which can be either MFM or Manchester at a maximum data rate of 5 Mbit/s on a shared media (physical bus). The pins can either be connected to drivers using recessive/dominant states on the wire as well as drivers using active push/pull functionality.

The RXD signal uses '1' as the inactivity level. In the so-called RS485 compatible mode longer periods of '0' are treated as inactivity, too. If the RS485 compatible mode is not used, the application must care to drive RXD to '1' during inactivity on the bus.

Pin Name	Mode	Connect to PHY	Comment
TXD[0]	out	TXD	Transmit data channel 0
CTS[0]	out	CTS	Transmit enable channel 0
TXCLK[0]	in		No function (do not connect)
RXER[0]	in		No function (do not connect)
RXCLK[0]	in		No function (do not connect)
RXDV[0]	in		No function (do not connect)
RXD[0]	in	RXD	Receive data channel 0
TXD[1]	out	TXD	Transmit data channel 1
CTS[1]	out	CTS	Transmit enable channel 1
TXCLK[1]	in		No function (do not connect)
RXER[1]	in		No function (do not connect)
RXCLK[1]	in		No function (do not connect)
RXDV[1]	in		No function (do not connect)
RXD[1]	in	RXD	Receive data channel 1

TTP/C Synchronous Bus Interface

When in synchronous mode of operation, the bus unit uses a synchronous transfer method to transfer data at a rate between 5 and 25 Mbit/s. The interface is designed to run at 25 Mbit/s and to be gluelessly compatible with the commercial 100 Mbit/s Ethernet MII (Media Independent Interface) according to IEEE standard 802.3 (Ethernet CSMA/CD).

Connecting the synchronous TTP bus unit to a 100 Mbit/s Ethernet PHY is done by connecting TXD, CTS, TXCLK, RXER, RXCLK, RXDV and RXD of any channel to TXD0, TXEN, TXCLK, RXER, RXCLK, RXDV and RXD0 of the PHY's MII. The pins TXD1, TXD2 and TXD3 of the PHY's MII should be linked to VSS. The signals RXD1, RXD2, RXD3, COL and CRS as well as the MMII (Management Interface) should be left open or can be used for diagnostic purposes by the application.

Note that the frames sent by the AS8202NF are not Ethernet compatible and that an Ethernet Hub (not a Switch) can be used as a 'star coupler' for proper operation. Also note that the Ethernet PHY must be configured for Full Duplex operation (even though the Hub does not support full duplex), because TTP has its own collision management that should not interfere with the PHY's Half-Duplex collision management. In general, the PHY must not be configured for automatic configuration ('Auto negotiation') but be hard-configured for 100 Mbit/s, Full Duplex operation. Note that to run the interface at a rate other than 25 Mbit/s other transceiver PHY components have to be used.

Pin Name	Mode	Connect to PHY	Comment
TXD[0]	out	TXD0	Transmit data channel 0
CTS[0]	out	TXEN	Transmit enable channel 0
TXCLK[0]	in	TXCLK	Transmit clock channel 0
RXER[0]	in	RXER	Receive error channel 0
RXCLK[0]	in	RXCLK	Receive clock channel 0
RXDV[0]	in	RXDV	Receive data valid channel 0
RXD[0]	in	RXD0	Receive data channel 0
TXD[1]	out	TXD0	Transmit data channel 1
CTS[1]	out	TXEN	Transmit enable channel 1
TXCLK[1]	in	TXCLK	Transmit clock channel 1
RXER[1]	in	RXER	Receive error channel 1
RXCLK[1]	in	RXCLK	Receive clock channel 1
RXDV[1]	in	RXDV	Receive data valid channel 1
RXD[1]	in	RXD0	Receive data channel 1

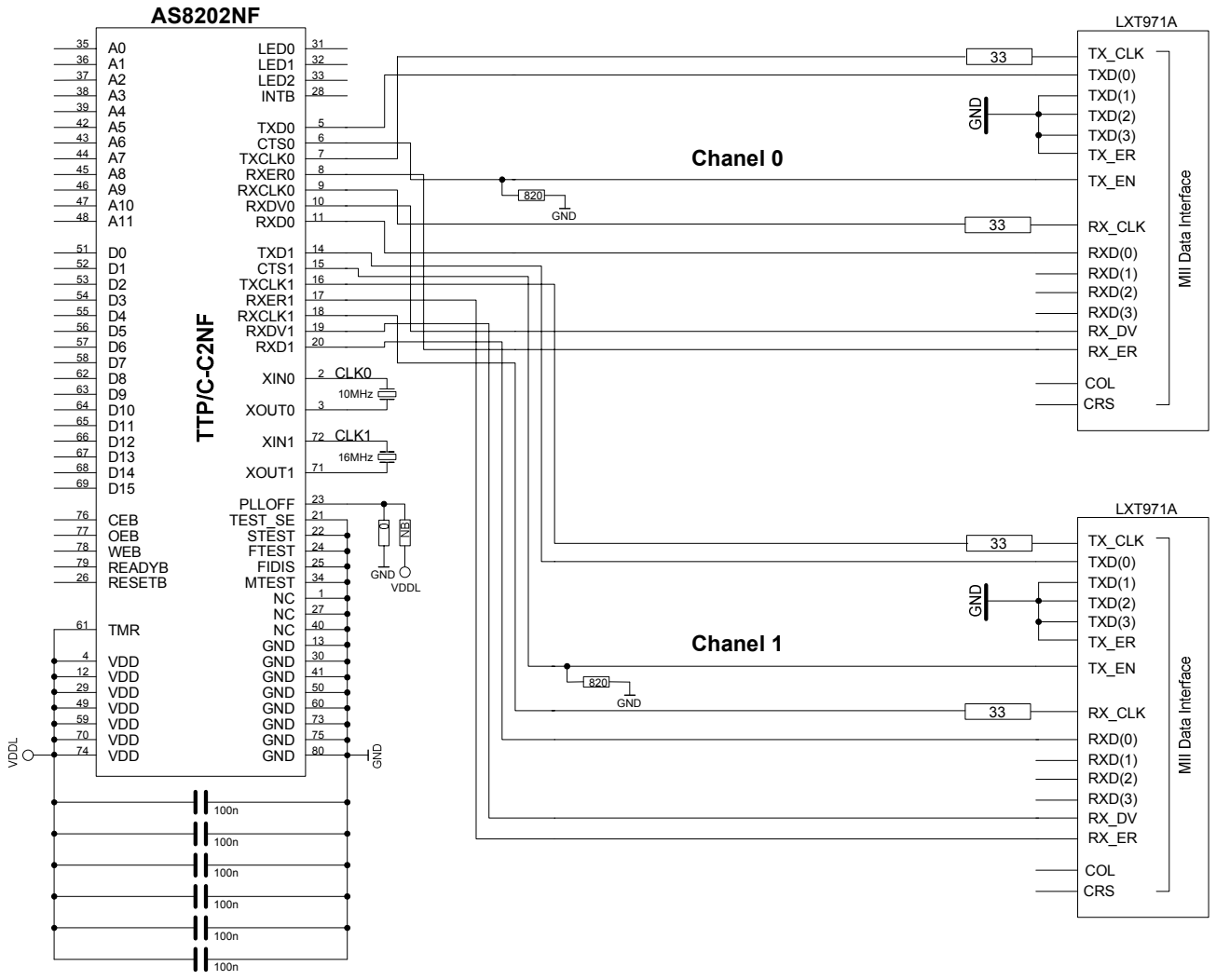

Figure 1. AS8202NF Connected to LXT971A (MII Interface)

Intel LXT971A is an IEEE compliant Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). The LXT971A also provides a pseudo-ECL (PECL) interface for use with 100BASE-FX fiber networks.

The LXT971A supports full-duplex operation at 10 Mbps and 100 Mbps. Its operating condition can be set using auto-negotiation, parallel detection, or manual control. For more information see *LXT971A/972A 3.3V PHY Transceivers Design and Layout Guide (Application Note November 2001).*