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Title: Host Read Accesses Speedup in AS8202NF

Related Revision: Datasheet rev. V0.6 and later

Itroduction:

According to AS8202NF datasheet (from V0.6) the host access for successive read operations has to be separated by at least 37.5 ns (See AS8202NF datasheet V0.6 or newer, Asynchronous DPRAM Interface, Symbol 16, host read access inactivity time). In certain situations this inactivity time can be reduced significantly to improve the timing.

This document is intended to help designing glueless and high-speed connection between the host and the AS8202NF by explaining in which situations an inactivity time of as small as 5 ns can be used between successive read operations and how to avoid the remaining situations when the default timing is required.

Description:

Following a read access that is

- not from a register location (word address 0x000 to 0x013),
- not from a read-protected memory address and
- not from the last memory location in a selected page (word address 0x7FF or 0xFFF),

the next read access can be started after an inactivity time (the time when CEB or OEB or both is in the inactive state) of 5 ns. This drasticly speeds up the data transfer from the chip to the host for memory (frame) transfers if the application designer is able to handle the special cases appropriately.

Action Points:

To speed up the host read access one of two options can be implemented:

1. Using the READYB signal, the following requirements have to be met:

a) Set up the system's read access inactivity time to a minimum of 5 ns (between successive read accesses either CEB or OEB or both must be in the inactive state for a minimum duration of 5 ns).

b) In the application software assure that there is no read access to read-protected memory locations. Note that read protection is only active when the controller is switched on - this means, that, for example, checking memory areas when the controller is switched off can be performed even if a part or all of this memory is read protected when the controller is switched on.

c) In the application software assure that there is a minimum of 37.5 ns between two successive register accesses or between a register access and a memory area access. This can be done either by verifying that the host does never read from the AS8202NF within 37.5 ns after a register read access or by inserting a dummy write access to the AS8202NF after each register read access. If implemented, the dummy write access should write a random value to register location 0x013 (the write access is ignored by the AS8202NF but allows the timing to be met).

d) Carefully consider or avoid the use of functionality that speeds up read accesses, for example read-ahead logic.

e) In the application software assure that after reading the last word of a page (by accessing memory location 0x7FF or 0xFFF) there is no successive read access to the AS8202NF within 37.5 ns. This can be done as noted under c). If meeting this timing can not be guaranteed, the last word of each page has to be spared from the schedule (MEDL) so that the application software never reads data from these CNI addresses.

2. Not using the READYB signal

If READYB is not used by the application, the host has to assure that it applies CEB, OEB and WEB for a time that is long enough for the read/write access to finish. If this access mode is set up correctly, the read inactivity time can be reduced to 5 ns. Please note that in that case the application environment has to ignore the READYB signal completely.

Revision history:

1.0->1.1: Added option 2 for not using the READYB signal