Appnote Phys Layer for TTP/C
Setting of Delay Correction
Author:　　　**Wolfgang Dittrich & Ivan Rajkovic**
Date:　　　　**01-08-2003**

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MFM Physical Layer for TTP/C Appnote:
Calculating Time Skew Requirements

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1. Preface

1.1.   Objective of this document:

This document specifies the basic timing requirements for the MFM coded physical layer (PHY) for TTP/C. It describes the timing requirements without application specific details. The time-triggered protocol meets the requirements for safety critical distributed real-time systems in application domains like automotive, aerospace and industrial control electronics. The physical layer must provide a robust data transmission in severe environment with high noise levels. This document should help design engineers with the PHY considerations during the system design and provide a term definition which should also ease the customer support.

1.2.   What is included in this document?

All TTP/C specific requirements and limits for MFM physical layer. Some requirements must be specified for the system (i.e. temperature requirement) by the car, aircraft or system manufacturer. Only the method (method of overtemperature protection) is described in this document.
It is the responsibility of the car, aircraft or system manufacturer to define the system parameters depending on application and environment-specific requirements.

1.3.   What is not included in this document?

The following spec intentionally does not deal with application specific requirements. Diagnostic features for instance will be a big demand for all car manufacturers, but no TTP-requirement. What is monitoring and which interface to use for that purpose is to be defined by the car manufacturer. For aircraft or industrial use there will be different requirements.

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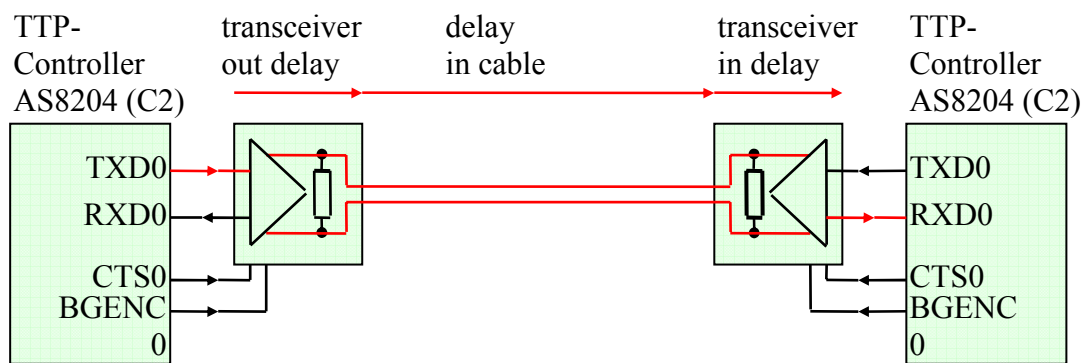Date: **01-08-2003**

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2. Theoretical Considerations

The following chapter offers the definition of terms used during the PHY design, theoretical considerations and some numerical examples

2.1.   Definition of Delays

Looking at 2 nodes, the signal flow looks like this
(for example, on channel 0, with C2S-controller):

The signal flow will experience 3 different delays. These delays must be specified individually to be compensated in the "delay correction term" in the MEDL, that denotes the expected delay of signal propagation between two nodes.
Also there will be a difference between rising and falling edge propagation delay when being processed in the transceivers.
The sum of all delays will split into:
-    "symmetric" delay:
     falling and rising adges are delayed with the same value (i.e. dielectric delay in the cable)
-    "asymmetric" delay:
     falling and rising adges are delayed with a small differenc due to not perfectly symmetric behavior of the transceivers. This is called "time skew". There is a requirement for maximum allowed time skew to guarantee proper operation of the MFM-Decoder.

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2.2. Calculating Maximum Time Skew for Proper Operation:

Both transceivers in the signal flow will add some distortion that means the propagation delay of rising and falling edge will not be exactly the same. There is a maximum amount of time skew for proper decoding of the MFM modulated data string. You will find this in the corresponding data sheet.

After the theoretical considerations there will be shown an example for calculation with following parameters:

- controller chip   AS8204 (CMOS Process)
- bit rate   5Mbit/s
- quartz clock   10MHz
- internal clock   80MHz (PLL factor 8)

For the calculations of the acceptable degradation of the time margin, we use the assumption, that there is no propagation delay in the transmission line. This assumption is non restrictive, because this is a fundamental task of the TTP protocol itself.

The allowed Time Span ($T_{time-span}$) will be reduced due to the asymmetric delay (positive or negative) of two logical parts: logical delay caused through the phase noise (jitter) of the PLL based frequency multiplier ($T_{logicai-skew}$) and physical asymmetric delay ($T_{physcal-skew}$):

$$T_{total-skew} = T_{logical-skew} + T_{physical-skew},$$
so that we can postulate following equation:
$$T_{time-span} = T_{total-skew} + \Delta_t,$$
where Δ_t is a allowed time margin, which has to be specified by the designer.

We use the term skew for the asymmetric delay because of the non constant (random) nature of the delay, which is always different from cycle to cycle.

The physical skew is technology determined, for instance for the CMOS type transceivers are the rising edge and falling edge slew rate different due to the unequal $r_{dson,p}$ and $r_{dson,n}$ of the output buffer. We use the conservative equation for the physical skew
$$T_{physical-skew} = \max(t_{PLH}, t_{PHL})$$

These parameters (t_{PLH}, t_{PHL}) are usually found in the datasheets of the product, although for nominal pin load. In concrete cases the rising edge and falling edge slew rate will be determined through the actual pin load and should therefore be measured. It should be noted that for the following calculation the double value for the physical skew should be used, due to the splitting into logical and physical skew and there exist two sources of physical skew, on the receiver and on the transmitter, respectively.

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The logical skew is far more complicated to estimate, due to the random nature of the process. But first we have to present a recommendation for a mathematical treatment which will describe the jitter behaviour of the internal clock.

It is a common practice (due to the EMC regulations) to have a relatively slow clock oscillator on the board and to generate the working frequency with a frequency multiplier (typically a PLL). The major drawback of this approach is greatly enhanced short term instability of the working frequency compared with the slow reference clock. The internal clock period (T_{CLP}) can be calculated as follows:
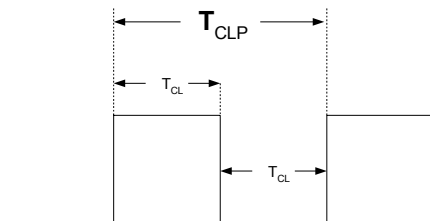
$$T_{CLP} = (\frac{1}{N_{PLL}} \bullet T_{OSZ}) \bullet \alpha_X$$

$N_{PLL} = 1,2,4,8$ the internal PLL multiplying factor

$T_{OSZ} = \dfrac{1}{f_{OSZ}}$ the oscillator period of the board reference clock

$\alpha_X = (1-\theta, 1+\theta)$ Statistical correction factor for jitter modelling, also known as sideband noise correction factor

θ $\pm$(½ Jitter value[in UI – see further text])

The statistical correction factor models the jitter in the output clock; there are 3 major jitter sources:

- amplified jitter of the reference clock
- jitter due to the power supply fluctuations
- intrinsic residual jitter from the PLL circuit itself

It is important to understand that the jitter is stochastic in nature and you may describe it only as a random variable with respect to time.

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You can quantitatively express jitter in the following ways:
- In unit intervals (UI). One UI is one cycle of the clock frequency, which is the normalized clock period. Jitter expressed in UIs describes the magnitude of the jitter as a decimal fraction of one UI
- In degrees. Jitter expressed in degrees describes the magnitude of the jitter in units of degree for which one cycle equals 360.
- In absolute time. Jitter expressed in units of time describes the magnitude of the jitter in appropriate orders of magnitude – typically ps.
- As a power measurement in units of radians or unit intervals squared, which is often expressed in decibels

All these quantifications of jitter describe a worst case clock-to-clock jitter. The low frequency wander is not modelled with this description. Also, it is to expect that a k-cycle jitter tends to be smaller as k increases. Typically, you will be needing both values: a clock-to-clock jitter and a k-cycle jitter for a realistic jitter estimation. Fortunately, most ASIC vendors enclose the numeric data describing the output jitter in their data sheets. If this is not the case you should consider the jitter measurement technique described in Reference [1].

Due to the clock output jitter there comes to changes in the pulse width of the pulse: the pulse width boundaries can be calculated through:

$$T_{logical-skew} = m \cdot (T_{CLPt(nom)} - T_{CLPt(\min/\max)}) \, ,$$

where

$T_{CLPt(nom)}$ — The nominal output clock frequency of the transmitter

m — The oversampling ratio of the transmitter controller

$T_{CLPt(\min/\max)}$ — The shortest and the longest impulse, calculated with m-cycle jitter correction factor

For a MFM coded system the maximum allowed time skew on the RXD pins is:

$$T_{time-span} \in (-n \cdot T_{CL\Pr} + T_{physical-skew}, n \cdot T_{CL\Pr} - T_{physical-skew})$$

where

$n = 3$ — for 16 times oversampling

$n = 2$ — for 8 times oversampling [(see HDD_MFM_receiver_stage.doc)]

With these considerations we can calculate the allowed Time margin Δ_t :

$$\Delta_t = T_{time-span} - T_{total-skew}$$

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2.3. Numerical Example

In the following chapter we will present two calculation examples for typical system parameters, as presented in preceding chapter (bit rate 5MHz) and for a system with a lower bit rate of 500 kHz.

2.3.1. System with a bit rate of 5 MHz

For system with given parameters (see previous chapter) the nominal clock period can be calculated as

$$T_{CLPt(nom)} = (\frac{1}{N_{PLL}} \cdot T_{OSZ}) = \frac{1}{8} \cdot 100ns = 12.5ns .$$

For the 16 times oversampling we use for the oscillator sideband noise correction factor $\alpha_x = (0.96, 1.04)$ (empirical value), which yields

$$T_{CLP(min)} = 12.5ns \cdot 0.96 = 12ns ,$$

so that we can calculate

$$T_{logical-skew} = m \bullet (T_{CLPt(nom)} - T_{CLPt(min/max)}) = 16 \cdot 0.5ns = 8ns .$$

Since system uses MFM coding it is allowed to use for the calculation of the time span

$$T_{time-span} \in (-3 \cdot 12ns + 4ns, 3 \cdot 12ns - 4ns) \Rightarrow T_{time-span} \in (-32ns, 32ns) ,$$

which yields for the time span

$$\Delta_t = T_{time-span} - T_{total-skew} = 32ns - 8ns = 24ns \Rightarrow \Delta_t = \pm 24ns$$

2.3.2. System with a bit rate 500 kHz

For this calculation we use very simple system with a 500 kHz bit rate. Compared with the preceding example we can neglect the influence of the clock jitter if we postulate the same clock frequency. In this case we have (since logical skew equals zero):

$$\Delta_t = T_{time-span} = 3 \cdot 125ns - 4ns = 371ns \Rightarrow \Delta_t = \pm 371ns$$

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3. References

[1.] High – Speed Digital Design – On line Newsletter by Dr. H. Johnson, Vol. 3. Issue 22, http://signalintegrity.com/Pubs%5CNews%53C_22.htm