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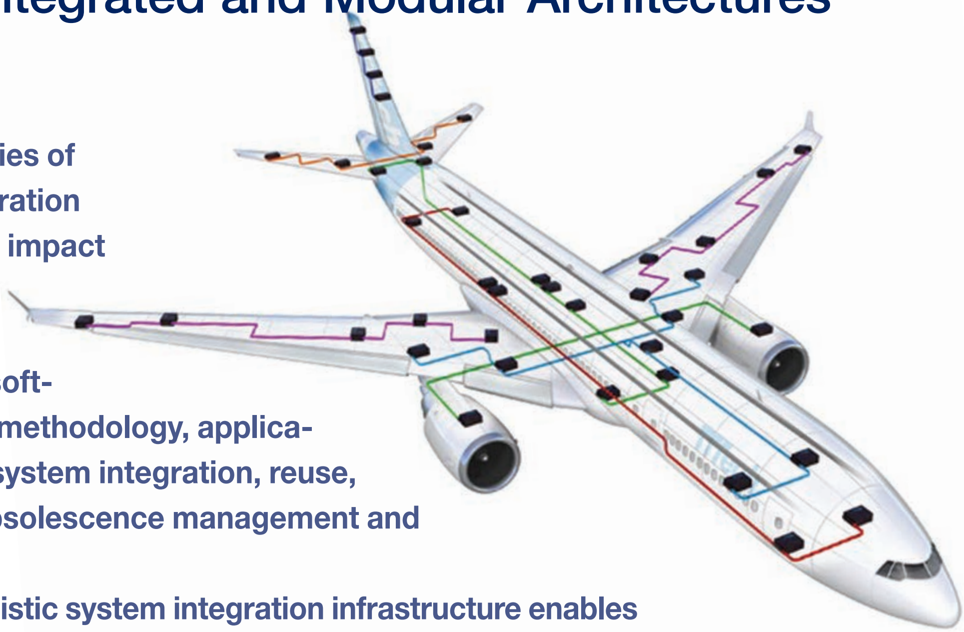
TECH REPORT

Deterministic Networks for Advanced Integrated Systems

Deterministic Ethernet and TTP Networks for Integrated and Modular Architectures



The capabilities of system integration technologies impact electronics platform complexity, software design methodology, application design, system integration, reuse, upgrades, obsolescence management and certification.

The deterministic system integration infrastructure enables design of less complex software-centric systems, robust by-wire controls and integrated modular architectures at lower lifecycle cost. TTP network and deterministic Ethernet (ARINC 664/AFDX, TTEthernet) product lines by TTTech are suited for a broad range of demanding avionics and vetronics architectures targeting minimized system complexity and reduced size, weight and power (SWaP).

Access Intelligence

Deterministic Networks

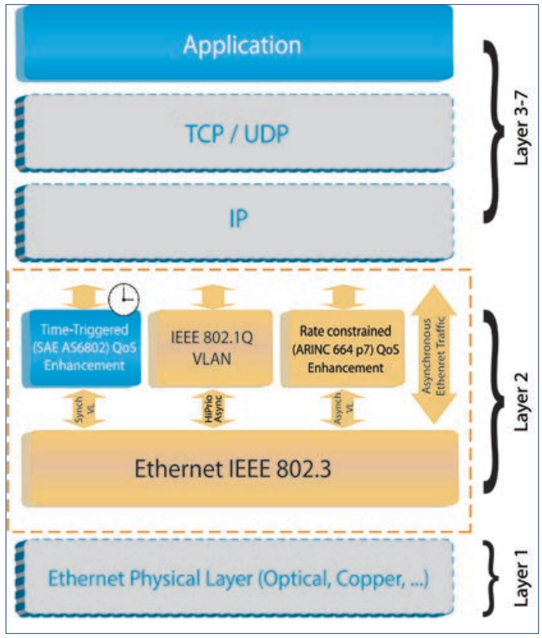
Time-triggered communication relies on robust fault-tolerant synchronization, tight control of jitter, TDMA communication and scheduled exchange of message frames. The operational principle can be applied to fieldbuses or Ethernet networks to ensure synchronized operation of integrated modules, fixed communication and microsecond jitter.

Strictly deterministic TTP networks (based on open SAE AS6003 “TTP Communication Protocol” standard) are designed for safety-critical, by-wire applications, with bandwidth of up to 20Mbit/s per channel and available on the market since 2001. TTP has been applied in key integrated systems for more electric aircraft, distributed power generation, engine and flight controls. Modular distributed systems which are integrated by TTP are in Airbus A380, Boeing 787, Bombardier CSeries, Embraer Legacy, fighter jets and other regional and business aircraft.

With capabilities for deterministic high-bandwidth communication standardized recently (ARINC 664 Part 7 (AFDX) and SAE AS6802 “Time-Triggered Ethernet”), the Ethernet is becoming widely used as aircraft backbone network, and its application helps to design novel optimized systems and architectures in modern, more electric’ aircraft. Deterministic Ethernet networks provide congestion-free, real-time Ethernet traffic with all necessary QoS services required for design of critical integrated systems. This helps to design embedded architectures with gigabits of available network bandwidth and high-speed controls.

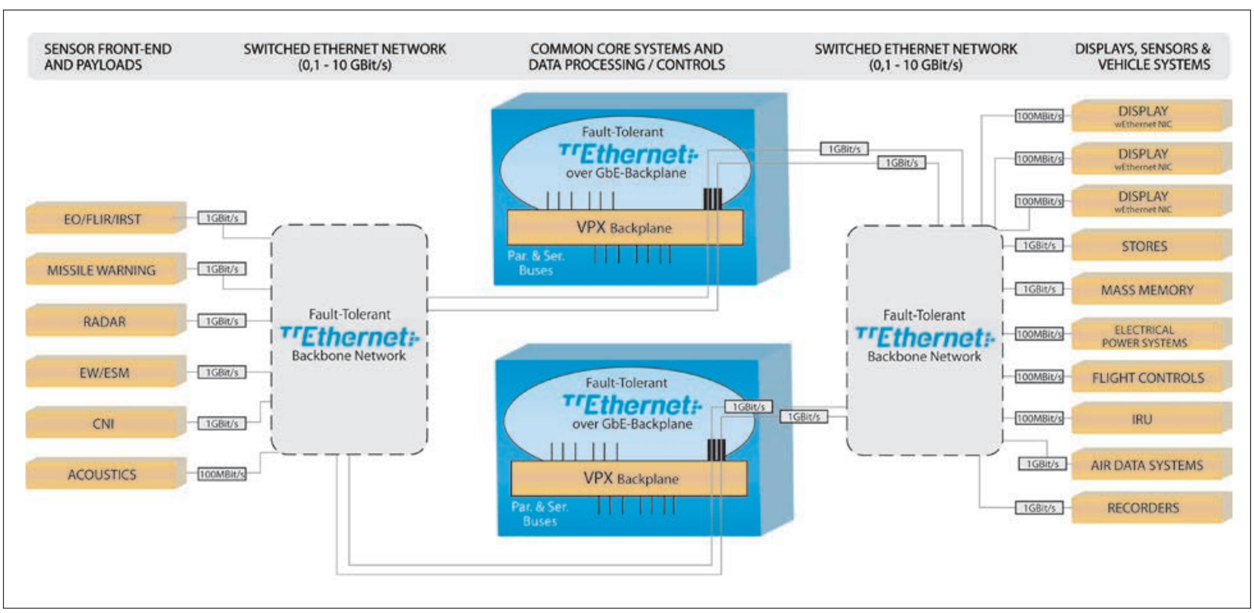
Deterministic Ethernet with Layer 2 Quality-of-Service Enhancements

Ethernet is a family of frame-based communication standards and a versatile networking technology, which enjoys tremendous support in various commercial and industry applications. It relies on asynchronous communication and statistical bandwidth multiplexing which imposes severe constraints on resource sharing and deterministic, real-time operation in complex distributed systems. This has severely limited design of advanced integrated systems in the past. Fortunately, the capabilities of Ethernet can be expanded by additional Layer 2 Quality of Service (QoS) enhancements implemented on a switch or network interface.



TTEthernet switch provides time-triggered (synchronous), rate-constrained and regular Ethernet traffic class.

QoS enhancements for Ethernet such as ARINC 664 Part 7 (AFDX), and SAE AS6802 “Time-Triggered Ethernet” guarantee deterministic computing and networking performance for time-, mission-, and safety-critical functions in advanced Ethernet-based integrated systems. The both open standards are integrated on DO-254 compliant Ethernet switch product line



Deterministic Ethernet as backplane/backbone network enables design of advanced integrated systems and architectures.

TTEthernet provided by TTTech.

SAE AS6802 (TTEthernet) and ARINC 664-P7 target similar challenges in avionics design, but use very different operation principles. Time-triggered messages are driven by the progression of time, while ARINC 664-P7 relies on asynchronous rate-constrained communication with defined maximum latency. Both services define Virtual links (VL) for communication (see table below). All higher layers and applications can simply select a traffic class required for particular distributed applications.

Backbone and Backplane Ethernet Networks

SAE AS6802 traffic class complements ARINC 664-P7 capabilities with strictly deterministic behavior. Time-critical (hard real-time) applications, audio and video can be easily integrated into large ARINC 664-P7 networks using time-triggered messages, without influencing other distributed functions integrated in the network.

DO-254 compliant TTEthernet switches enable hard real-time messaging, redundant networking, and full support of ARINC 664-P7 (AFDX) protocol services for avionics, vetronics and critical control architectures. Time-triggered QoS enhancements (SAE AS6802), implemented on TTEthernet switch products, satisfy requirements of backplane and backbone Ethernet applications in aerospace, automotive, energy production and industrial systems. TTEthernet switches can be used for both high-speed backbone and switched fabrics (backplane) in modular racks (e.g., VPX, ATCA or similar) and design of generic open architectures using a broad selection of embedded COTS boards.

TTEthernet switch modules are suitable for application in commercial aircraft systems, and offer an extended set of networking capabilities for time-, mission-, and safety-critical applications and integrated modular avionics (IMA) architectures. The latest product developments target design of VPX-based systems which rely on TTEthernet switch capabilities to integrate payloads, core common computing systems and mission computers with all vehicle systems, where all sensor and effector data and can be easily accessible for distributed processing functions.

Advanced ARINC664 (AFDX) Switching

In addition, TTEthernet switches simplify the integration and alignment of functions relying solely on ARINC664 virtual links. With robust system synchronization for application tasks, provided in SAE AS6802 services, the system designer can align functions for hard real-time control tasks even if time-triggered Ethernet traffic class is not used.

By configuring and using only ARINC 664 functions of TTEthernet devices, system architects can use it as a DO-254 compliant AFDX switches and end systems.

Reducing System Complexity with Deterministic Networks

By providing unambiguous definition of temporal behavior and key system interfaces at the network level, time-triggered services in TTP and TTEthernet networks support less complex distributed computing and networking, enhance resource sharing (or separation) among critical and non-critical functions, and simplify coordination of critical functions. With TTP (AS6003) networks and SAE AS6802 services for Ethernet, it is possible to emulate

		Deterministic Networks		
		Deterministic Fieldbus	Deterministic Ethernet	
Communication Network	**Switched IEEE802.3 Ethernet**	**TTP (AS6003) Network Devices**	**AFDX / ARINC 664 p7 Network Devices and Switches**	**Ethernet switch with SAE AS6802 (TTEthernet® Network Devices and Switches)**
Media Access	Full Duplex, Switched	Scheduled communication, TDMA	Full Duplex, Switched	Full Duplex, Switched, Scheduled (TDMA) for AS6802 traffic class
Bandwidth	100 MBit/s, 1 Gbit/s, and higher	up to 5 MBit/s (BUS), 20 Mbit/s (STAR) per channel, single or dual-channel	100 MBit/s - 1Gbit/s	>100 MBit/s, 1 Gbit/s, and higher
Topology	Star	Bus (Star)	Star	Star (Line, Mesh)
Physcial Layer	wired IEEE 802.3 physical layers	up to 5 MBit/s (RS-485 or MIL-1553), for 20Mbit/s (Ethernet 100BASE-T, MII)	wired IEEE 802.3 physical layers	wired IEEE 802.3 physical layers
Bandwidth Partitioning	Statistical multiplexing	TDMA	Statistical multiplexing with rate-constrained messaging and traffic policing for AFDX® traffic	- TDMA for scheduled Ethernet traffic, - Statistical multiplexing for best-effort and/or ARINC 664 p7 traffic (see AFDX®)
Determinism	**Non-Deterministic:** Best Effort* *) "more deterministic" with VLAN IEEE802.1Q	**Strictly Deterministic:** Defined Fixed Latency, µs-Jitter and Message Order	**Very Deterministic:** Defined maximum latecy for all Virtual Links (VLs)	**Strictly Deterministic:** Defined Fixed Latency, µs-Jitter, Message Order for all scheduled Virtual Links (VLs)* **) Allows asynchronous bulk and rate-constrained (ARINC 664 p7) data transfers in parallel*
Frame size	64 - 1522 Byte	max. 248 Bytes	64 - 1518 Byte	64 - 1522 Byte
Redundancy	No	Dual-redundant communication channels	Dual-Redundant communication	simplex, 2-, 3-, ..., N-x redundant communication
Fault Tolerant System Clock	No	Yes	No	Yes
Real-Time	Limited	Yes	Yes	Yes
Hard Real-Time	No	Yes	Limited	Yes
Asynchronous and Synchronous Traffic	No	No	No	Yes
Target Application	Standard LAN	Modular Controls and Deterministic By-Wire Systems	Deterministic Backbone, IMA 1G, Core Avionics Systems, Modular Controls, By-Wire Controls	Deterministic Backbone, IMA 1G/2G (distributed IMA), Cyber-Physical Systems, Core Avionics Systems, Ultra Fast By-Wire Controls, Modular Controls, High-Integrity Architectures

Comparison: Deterministic Ethernet and TTP Standards

conflict-free shared system memory via periodic and synchronized global data exchange to guarantee high levels of software abstraction. This minimizes application design effort, code size, and exposure to transient faults or unintended system states.

Advanced Integrated Architectures

System architecture design decisions are influenced by available network technologies and there is a direct link between communication network capabilities, related complexity and lower system life-cycle cost for advanced integrated systems. For example, the lack of robust bandwidth partitioning and the capability to run both hard real-time controls and less demanding real-time or soft time functions, either mandates separation of physical resources and design of hierarchical architectures, or limits efficient use of computing resources and functional alignment.

In a case where system integration allows placement of functions anywhere in the vehicle or aircraft without impact on function performance, there are countless opportunities to design more SWaP-efficient systems and architectures.

Deterministic Ethernet and TTP networks help designers to resolve many system integration and architecture challenges, and design more efficient and optimized integrated systems.