

TTEEnd System A664 Core IP Pro Integration Kit

Ready to Run Kit for Certifiable TTEthernet End System A664 Core IP Pro



Key Benefits

- Integration example for DO-254 DAL A certifiable ^{TTE}End System A664 Core IP Pro.
- Time saving with simple out-of-the-box setup and comprehensive user and integration manuals.
- Cost saving with a pre-configured hardware and software development environment.

^{TTE}End System A664 Core IP Pro Integration Kit helps to avoid the time consuming and costly process of acquiring and integrating hardware and software components from different vendors. This out-of-the-box product provides a ready to use integration example for DO-254 DAL A certifiable ^{TTE}End System A664 Core IP Pro with pre-configured hardware and software development environment.

Three traffic classes on one chip

^{TTE}End System A664 Core IP Pro Integration Kit supports three Ethernet traffic classes:

- Standard (IEEE 802.3) traffic
- Rate Constrained (ARINC 664 part 7) traffic
- Time-triggered (SAE AS6802A) traffic

Integrated platform for development

^{TTE}End System A664 Core IP Pro is delivered as a high-end netlist wrapped by peripheral IP blocks to provide a functional End System example. It is demonstrated on a Xilinx Zynq UltraScale+ MPSoC FPGA that communicates with the Host computer via PCIe interface and the Ethernet network via two redundant 100/1000 Mbit/s channels with RGMII interface.

Up to 1 Gbit/s of safety-critical traffic

TTEEnd System A664 Core IP Pro supports the transmission of all three traffic classes over the network with up to 1 Gbit/s speeds in a deterministic way. Additionally, the SAE AS6802A traffic class provides fixed transmission latency and jitter in the sub-microsecond range and unmatched bandwidth efficiency while maintaining full determinism (up to 95% utilization of available network bandwidth). The redundant Ethernet network interface allow the integration of TTEEnd System A664 Core IP in fault-tolerant networks.

SWaP Optimization

The possibility to utilize MPSoC platforms allows the integration of the ^{TTE}End System A664 Core IP Pro solution on high circuitry density PCBs. This provides flexibility in the hardware design and leads to significant SWaP improvements.

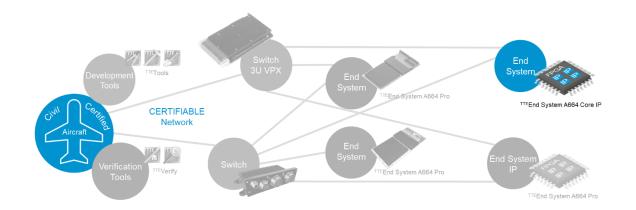






Application Fields

- Technology evaluation
- Architecture
- developmentFlight programs



General Product Features	 Ready to run integration example for DO-254 DAL A certifiable ^{TTE}End System A664 Core IP Pro End System Core IP netlist for Xilinx US+ Family (Development License) 256 Tx VLs 512 Rx VLs 2,048 Tx ports 4,096 Rx ports Example Peripheral IP in RTL Pre-compiled End System IP as bitstream Demo application software (source code)
Hardware	 Zynq UltraScale+ MPSoC ZCU106 Evaluation Kit 4-port Gigabit Ethernet FPGA mezzanine card (FMC)
Standards Compliance	 IEEE 802.3 ARINC 664 part 7 SAE AS6802A
Interfaces	 Zynq UltraScale+ MPSoC ZCU106 Host interface: PCIe® 3.0 x4 Network interface: supports two RGMII channels ^{TTE}End System A664 Core IP Pro Host interface: AXI4, 32-bit at 125 MHz Network interface: supports two GMII channels
Documentation	 User & integration manuals
Drivers (non-certified) support	 TTE-COM Driver middleware image for Linux Ubuntu 20.04 Other driver options upon request
Order Number	- 13380
Tools Support	 TTETools Development Suite – for device configuration creation
Related Products	 13869 - ^{TTE}End System A664 Core IP Pro Certification Data Package, Project License 13056 - ^{TTE}Tools 5 Development Suite - Starter Edition 13823 - Integration support



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